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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/620,045	07/15/2003	Rajarshi Bhattacharya	1-4-2-2-1	7529

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EXAMINER	
JACOB, MARY C	

ART UNIT	PAPER NUMBER
2123	

DATE MAILED: 06/19/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/620,045	BHATTACHARYA ET AL.	
	Examiner	Art Unit	
	Mary C. Jacob	2123	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *15 July 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-19* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-19* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *9/5/03* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *12/16/03*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1-19 have been presented for examination.

Specification

2. The disclosure is objected to because of the following informalities. Appropriate correction is required.

3. Page 1, line 7 and Page 10, line 23-24 refer to US Patent Applications by the corresponding Attorney Docket Numbers and should be replaced by the current application or patent number.

Claim Rejections - 35 USC § 102

4. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

5. Claims 1, 2, 6, 7, 12-14, 16-19 are rejected under 35 U.S.C. 102(b) as being anticipated by Boggio et al ("NetworkDesigner-Artifex-OptSim: A Suite of Integrated Software Tools for Synthesis and Analysis of High Speed Networks", Optical Networks Magazine, September/October 2001).

6. As to Claims 1, 16, 18 and 19 Boggio et al teaches: a method of simulating the operation of an electronic system comprising a plurality of circuit elements, utilizing a software-based development tool, the method comprising the steps of: providing in the

software-based development tool an interface permitting user control of one or more configurable parameters of the electronic system (page 28, column 2, 4th and 5th bullets; page 29, section 2, paragraph 3); and automatically generating a simulation configuration for the electronic system based on current values of the configurable parameters, the simulation configuration being generated without requiring further user input, the simulation configuration specifying interconnections between the circuit elements which satisfy the current values of the configurable parameters (page 30, column 1, lines 7-15). As to the storage, memory and processing device, since Boggio et al is directed to software tools running simulations including a debugger, report generator (page 30, column 1, lines 44-46), libraries (Figure 1, "Equipment Library") and displaying output on a graphical user interface (Figure 12), it is understood that the software development tool must run on a computer system containing memory, processing device and a storage device.

7. As to Claim 2, Boggio et al teaches: wherein at least a subset of the circuit elements each comprise one or more integrated circuits (page 29, column 1, paragraph 5, sentence 3; page 30, column 2, lines 6-9).

8. As to Claim 6, Boggio et al teaches: wherein the interface includes a listing of the circuit elements and permits user control of one or more configurable parameters of each of the circuit elements (page 29, column 1, paragraph 5, sentence 3; page 30, column 1, lines 1-7).

9. As to Claim 7, Boggio et al teaches: wherein the interface includes a listing of a base device specified for the plurality of circuit elements and permits user control of one

or more configurable parameters of the base device (page 30, column 1, lines 1-7; page 10, column 2, lines 6-9).

10. As to Claim 12, Boggio et al teaches: wherein the software-based development tool comprises an automatic configuration generation module which generates the simulation configuration for the electronic system based on the current values of the configurable parameters (page 30, column 1, lines 7-15).

11. As to Claim 13, Boggio et al teaches: wherein the simulation configuration is generated utilizing an object-oriented programming construct comprising a base class, corresponding to a base device specified for the plurality of circuit elements, and an associated generation interface (page 30, column 1, lines 37-40; page 32, column 2, lines 27-35).

12. As to Claim 14, Boggio et al teaches: wherein the generation interface declares a generate function that is implemented by each of a plurality of generators, each of the plurality of generators corresponding to a different configuration of the electronic system (page 30, column 1, lines 7-15).

13. As to Claim 17, Boggio et al teaches: wherein the software-based development tool comprises a simulator control module (page 30, column 2, lines 3-5, 14-15), a set of interfaces (Figure 3; Figure 5; Figure 11), and circuit element modules each corresponding to an associated one of the circuit elements (column 30, lines 6-9).

Claim Rejections - 35 USC § 103

14. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

15. Claims 3, 4, 8, 9-11 and 15 are rejected under 35 U.S.C. 103(a) as being unpatentable over Boggio et al as applied to claim 1 above, and in view of Sun et al ("Simulation Studies of Multiplexing and Demultiplexing Performance in ATM Switch Fabrics", Performance Engineering in Telecommunications Network Teletraffic Symposium, 14-16 Apr 1993, pages 21/1 - 21/5).

16. As to Claims 3, 4, 8, 9-11 and 15, Boggio et al teaches a software development tool to automatically generate a simulation configuration based on user configurable parameters of circuit elements for the design and validation of optical networks (page

28, column 1, paragraph 1, column 2, paragraph 2 and bullet 4; page 30, column 1, lines 7-15).

17. Boggio et al does not expressly teach the network comprising a multistage switch fabric wherein the circuit elements comprise at least two ingress devices, at least one cross-connect device and at least two egress devices, wherein the configurable parameters comprise a number of ports of the electronic system, switching capacity, configuration type, such as one of a centralized configuration, stackable configuration or distributed configuration.

18. Sun et al teaches a method for modeling a switch fabric with basic components for simulation to study multiplexing and demultiplexing performance in a network, enabling the switch fabric to be modeled without losing generality (Abstract), wherein the electronic system comprises a multistage switch fabric, the circuit elements comprise at least two ingress devices, at least one cross-connect device and at least two egress devices (Figure 2 and description); wherein the configurable parameters comprise a number of ports of the electronic system (Abstract, sentence 2; page 21/1, paragraph 6, sentence 4 and 5; page 21/2, paragraph 3); a configuration type, use of a centralized configuration for a multistage switch fabric of the electronic system and the ability to build other configurations (Figure 2, page 21/3, paragraph 1), and switching capacity (Abstract, sentence 2; Figure 2; page 21/2, 3rd paragraph).

19. Sun et al and Boggio et al are analogous art since they are both directed to the modeling and simulation of a network.

20. It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the software development tool for an optical network as disclosed in Boggio et al to include the modeling of a multistage switch fabric wherein the circuit elements comprise at least two ingress devices, at least one cross-connect device and at least two egress devices, wherein the configurable parameters comprise a number of ports of the electronic system, switching capacity and configuration for a multistage switch fabric of the electronic system as taught in Sun et al since the method taught by Sun et al models a switch fabric for simulation and validation of a network without losing generality (Abstract).

21. Claim 5 is rejected under 35 U.S.C. 103(a) as being unpatentable over Boggio et al as applied to claim 1 above, in view of Ishida et al ("A 10-GHz 8-b Multiplexer/Demultiplexer Chip Set for the SONET STS-192 System", IEEE Journal of Solid-State Circuits, Vol. 26, No. 12, December 1991).

22. As to Claim 5, Boggio et al teaches a software development tool to automatically generate a simulation configuration based on user configurable parameters of circuit elements for the design and validation of optical networks (page 28, column 1, paragraph 1, column 2, paragraph 2 and bullet 4; page 30, column 1, lines 7-15).

23. Boggio et al does not expressly teach wherein the circuit elements comprise integrated circuits of a designated chip set utilizable in the electronic system.

24. Ishida et al teaches an ultra high speed 8-b multiplexer and demultiplexer chip set that has been developed for the synchronous optical network (SONET) as a key

component of next-generation optical fiber communication systems that will require higher data bit rates for future increases in transmission capacity (page 1936, column 1).

25. Boggio et al and Ishida et al are analogous art since they are both directed to the design of optical networks.

26. It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the design of the optical networks including user configurable parameters of circuit elements as taught by Boggio et al to include a chip set as taught in Ishida et al since Ishida et al teaches a high speed multiplexer and demultiplexer chip set that is a key component of a next-generation optical fiber communications systems that will require higher data bit rates for future increases in transmission capacity (page 1936, column 1).

Conclusion

27. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

28. Whitlock et al ("Simulation and Modeling: Simulating Optical Interconnects", IEEE Circuits and Devices Magazine, Volume 11, Issue 3, May 1995, pages 12-18) teaches an optical link simulator including a GUI and component models that are easily modifiable.

29. Wang et al ("A Distributed Switch Architecture with Dynamic Load-balancing and Parallel Input-Queued Crossbars for Terabit Switch Fabrics", IEEE INFOCOM 2002) teaches centralized and distributed switch architectures.

30. Chandhoke et al (U.S. Patent Application 10,200,091) teaches a prototyping device using a graphical user interface to allow the user to select operations to be included in the prototype, then creating the prototype without user intervention.

31. Peck et al (U.S. Patent Application 10,055,241) teaches a graphical user interface program that receives user input specifying a function and a configuration generation program generates a hardware configuration program based on the user input.

32. Cismas et al (U.S. Patent 6,996,799) teaches a system wherein hardware description language (e.g. Verilog or VHDL) and software language (e.g. C or C++) code for interconnecting cores is automatically generated by software tools from a central circuit specification.

33. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Mary C. Jacob whose telephone number is 571-272-6249. The examiner can normally be reached on M-F 7AM-5PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Paul Rodriguez can be reached on 571-272-3753. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

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6/7/06

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6/9/06